

Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Shokouhi (U.S. 6,249,458).

No claim has been amended. Claims 1-10 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the rejection of claims 1-10 under 103(a) as being unpatentable over AAPA in view of Shokouhi (U.S. 6,249,458) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

The present invention is in general related an electrostatic discharge (ESD) protection device as claim1 recites:

Claim 1. An electrostatic discharge (ESD) protection device, comprising:
an ESD protection circuit, comprising:
at least a diode connected in series between a first voltage and a pad; and
at least an ESD component connected in series between a second voltage and a pad, wherein *each of the at least an ESD component comprises a deep N-well region formed in a P-type substrate, a triple P-well formed in the deep N-well region, and a highly doped N-type (N+) region and a highly doped P-type (P+) region formed in the triple P-well region.*

The Office Action points out AAPA teaches forming the highly doped N-type region and highly doped P-type region in N-well region that is formed in a P-type substrate but fails to teach forming the highly doped N-type region and highly doped P-type region in a triple P-well located in a deep N-well region that is formed in a P-type substrate. Shokouhi et al. teach forming a device in a triple P-well located in a deep N-well region that is formed in a P-type substrate to limit or prevent leakage current. It would have been obvious to one skilled in the art of making semiconductor devices to incorporate the above teaching of Shokouhi et al. into the structure of AAPA to prevent leakage current.

However, in *claim 1* of the present invention, the highly doped N-type region and highly doped P-type region formed in a triple P-well located in a deep N-well region that is formed in a P-type substrate is *for reducing the parasitic capacitance and substrate noise of the ESD device.* The objective of the claimed invention is not limiting or preventing leakage current.

Shokouhi et al. teach the triple P-well resistor includes a central P-well region formed in a deep N-well that in turn is formed in a P-substrate. The N-well region is biased by a system

Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

voltage source (V_{cc}) and the P-substrate is grounded, thereby reverse biasing the central P-well region to limit leakage from the P-well region (col. 2, lines 41-50). In other words, *Shokouhi et al. disclose the device in a triple P-well located in a deep N-well region that is formed in a P-type substrate can limit or prevent leakage current, but Shokouhi et al. do not teach or suggest about reducing the parasitic capacitance and substrate noise.* Therefore, there is not any suggestion or motivation in the reference to one of ordinary skilled in the art, to combine the AAPA and Shokouhi's reference in a manner resulting in the claimed invention.

In addition, the device of Fig. 7 disclosed by Shokouhi et al. is *a triple P-well resistor including two P-doped regions 731, 733 in the triple P-well 730 formed in the deep N-well 720 that is formed in a P-substrate 710, and the deep N-well 720 is biased by a system voltage (V_{cc}) and the P-substrate 710 is grounded, thereby reverse biasing the central P-well region to limit leakage current from the P-well region.* However, the device in claim 1 is *an ESD component including a highly doped N-type region and a highly doped P-type region formed in a triple P-well located in a deep N-well region that is formed in a P-type substrate.* Apparently, the function and the structure of the device disclosed by Shokouhi et al. are much different from the ESD component of claim 1. Thus, there is not any suggestion or motivation in the reference to one of ordinary skilled in the art, to combine the AAPA and Shokouhi's reference in a manner resulting in the claimed invention.

Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patentably define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-10 patentably define over the prior art as a matter of law.

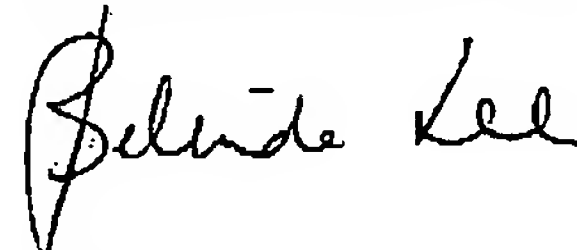
Customer No.: 31561
Application No.: 10/710,818
Docket NO.: 14217-US-PA-X

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: *Sept. 13, 2005*

Respectfully submitted,



Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jicgroup.com.tw
Usa@jicgroup.com.tw